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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,262	11/08/2001	Daniel Gudmunson	663-169/MBE	5008

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 07/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,262	GUDMUNSON ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 18-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 18-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
7/7/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arvind et al., Executing a Program on the MIT Tagged-Token Dataflow Architecture, 1990, IEEE, pages 300-3 18 (herein after "Arvind"), in view of Hennessy and Paterson, Computer Architecture A Quantative Approach, 1996, Morgan Kaufmann Publishers, Inc., Second Edition, pages 252-253 (herein after "Hennessy").

3. Referring to claim 1, Arvind have taught a method for data-driven synchronous parallel processing of a stream of data packets by multiple data processing units working in parallel, comprising the steps of:

a. distributing at least one instruction for data processing to one data processing unit of the multiple data processing units (page 303, firing an instruction);

b. storing the instruction in an execution instructions memory (Page 314, program memory);

c. sending from the one data processing unit a data request for at least one data packet corresponding to the instruction, required to execute the instruction (page 306, "read token" or "write token");

d. storing a record of the at least one data packet requested (page 306, waiting or deferred read request);

e. associating with the at least one data packet an address of the one data processing unit (pages 306, and 3 14-3 15, Section C. entitled "Multiprocessor Operation");

f. associating with the each data packet sent out a data token showing the readiness of the packet for further processing (Page 306, present, waiting, or deferred);

e. when the at least one data packet is received by the processing unit, associating the data packet with the corresponding instruction and distributing the data packet to the one data processing unit (page 306); and

g. processing the data according to the corresponding instruction (page 314, After the match occurs, the instruction is executed using the data.).

4. Arvind has not specifically taught "distributing at least one instruction for data processing to one data processing unit of the multiple data processing units, before the data processing unit is available to process the instruction". However reservation stations, as taught by Hennessy, are well known in the art to buffer instructions waiting to execute and buffer required operands and data as they become available (Hennessy, pages 252- 253), for the desirable purpose of executing the instructions as soon as all of the operands required for execution become available. This eliminates the need to retrieve the instructions and operands from registers at the time of execution, which speeds up instruction execution time. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the method of Arvind distribute at least one instruction for data processing to one data processing unit of the multiple data processing units, before the data processing unit is available to process the instruction, as

taught by Hennessy, for the desirable purpose of speeding up execution time by immediately executing instructions once all of the operands are available.

5. Referring to claim 2, Arvind and Hennessy have taught the method of claim 1, as described above, and wherein instructions are distributed to the multiple data processing units consecutively (Arvind, page 314, left hand column, Tokens enter the units in sequence; Hennessy, pages 252- 253).

6. Referring to claim 3, Arvind and Hennessy have taught the method of claim 1, as described above, and wherein instructions are distributed to the multiple data processing units concurrently (Arvind, page 303, left hand column, 5th paragraph).

7. Referring to claim 4, Arvind has taught the method of claim 1, as described above, and including, after step f., the step of putting the requested data packets into an internal data buffer in a data processing unit (Arvind, Page 314, WM).

8. Referring to claim 5, Arvind has taught the method of claim 1, as described above, and including, after step g., the step of erasing the record of the data request corresponding to the data packet (Page 314, When a match occurs a token is extracted.).

9. Referring to claim 6, Arvind has taught the method of claim 1, as described above, and including, during step g., the step of sending to the corresponding instruction in the execution instructions memory an indication that the at least one data packet has been received by the processing unit and is available for processing (page 314).

10. Referring to claim 7, Arvind has taught the method of claim 1, as described above, and including, during step e., the step of associating with the data packets an address of its sender and, during the step g, associating the data packet with the corresponding instruction according

to the address of the data packet sender (Page 314, Destination addresses are routed back to the top of the processing element.).

11. Referring to claim 8, Arvind has taught the method of claim 1, as described above, and including, during the step g, associating the data packet with the corresponding instruction according to the order of the data packet received (page 314, The data packets are associated as soon as they are received.).

12. Referring to claim 9, Arvind has taught the method of claim 4, as described above, and including the step of retrieving each data packet from the internal data buffer to be processed according to the corresponding instruction (Page 314, Tokens for the corresponding instruction are retrieved from the WM.).

13. Referring to claim 10, Arvind has taught the method of claim 1, as described above, and wherein an output of the processing step is sent to another data processing unit or out of the processor, or both (page 314, both).

14. Referring to claim 11, Arvind has taught the method of claim 1, as described above, and wherein processing occurs in real-time (Page 307, ID language is deterministic.).

15. Claim 28 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

16. Claims 18-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arvind, Executing a Program on the MIT Tagged-Token Dataflow Architecture, 1990, IEEE, pages 300-318 (herein after "Arvind").

17. Referring to claim 18, Arvind has taught an apparatus for substantially non-stalling data driven synchronous parallel processing of data packets including a digital data processor, further comprising:

a. an interface for receiving instructions and digital data from at least one external device and sending instructions or digital data or both to at least one external device (Page 3 14, Output tokens to network for another PE, page 303, tokens are tagged with instructions);

b. an instruction path contained inside the processor (Page 313-3 14, Instruction Fetch Unit uses an instruction path.);

c. a data path contained inside the processor; a plurality of data processing units organized for parallel processing of the data (Page 314, Paths to and from the WM.); and

d. a distributing unit organized for distributing one or more instructions at a time to the data processing units (Page 313-314, Figure 18, Instruction Fetch Unit).

18. Arvind has not taught that the data path is separate from the instruction path. However as an initial matter, making something separate is not a patentable difference (In Re Dulberg, 289 F.2d 522, 523, 129 USPQ 348,349 (CCPA 1961)). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the data path of Arvind, be separate from the instruction path, as it has been held that making something separable is not a patentable difference. Furthermore, this difference additionally would have been obvious to one of ordinary skill in the art at the time the invention was made. When the

path that instructions travel is a separate from the path that data travels, then no extra coding or tags are necessary to distinguish instructions from data when bits are read, i.e. instructions are read from an instruction path and data is read from a data path. (Referring to Figure 18 on page 313, there is an arrow from the program memory for the opcode, or instruction, and a separate arrow from the program memory for the data. These separate arrows strongly indicate that instructions and data each have their own separate paths.) Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instruction path of Arvind be separate from the data path of Arvind, such that no extra coding is necessary to distinguish instructions from data when bits are read from a path.

19. Claim 19 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

20. Claim 20 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

21. Referring to claim 21, Arvind has taught the apparatus of claim 18 wherein each data processing unit comprises

a. a storage for instructions (Page 314, right hand column, first paragraph, program memory);

b. a storage for records of outstanding data requests (Page 314, WM);

c. a storage for receiving requested data packets (Page 314, WM); and

d. a computation module for processing the requested data packets in accordance with at least one associated instruction (Page 314, Instruction Fetch Unit, ALU).

22. Referring to claim 22, Arvind has taught the apparatus of claim 21, as described above, and comprising control logic for controlling instruction and data flows through the processor (Figure 18, "Control").

23. Referring to claim 23, Arvind has taught the apparatus of claim 18, as described above, and wherein the digital data processor comprises a general-purpose microprocessor (abstract).

24. Referring to claim 24, Arvind has taught the apparatus of claim 18, as described above, and wherein the digital data processor comprises a graphics processor (Page 301).

25. Referring to claim 25, Arvind has taught the apparatus of claim 18, as described above, and wherein the digital data processor comprises a digital signal processor (abstract, page 301).

26. Referring to claim 26, Arvind has taught the apparatus of claim 21, as described above, and wherein the computational module operates using vector values (Page 301).

27. Referring to claim 27, Arvind has taught the apparatus of claim 21, as described above, and wherein the computational module operates using scalar values (Page 301, Where the vector size is 1.).

Response to Arguments

28. Applicant's arguments filed April 24, 2006 have been fully considered but they are not persuasive.

29. On pages 2 and 3, Applicant argues in essence:

> *"It is not possible in a purely data driven processor architecture such as Arvind et al. to distribute the instruction to a data processing unit before the data processing unit is available to process the instruction the way Hennessy does, since the processor does not at this stage know what instruction it must process."*
>
> However, Arvind does in fact know what instruction it must process. The known instruction pointer is stored in the wait match unit. Instructions are stored in a program

memory (page 314). When an entire block of code from the program memory is allocated to a PE, it is known where each instruction will be executed, since they are all executed in the same PE. So instructions can in fact be distributed to the data processing unit before the data processing unit is available to process the instruction by using a reservation station of Hennessy to serve as the rendevous point for matching up instruction data. Having the instructions be stored in a reservation station of Hennessy, at the PE of Arvind would have allowed the instruction to execute more rapidly once all of the data is ready. Therefore this argument is moot.

30. On page 3, lines 1-15, Applicant describes several different features and benefits of the present invention. It is noted that these features and benefits upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). If applicant would like specific feature read into the claims, then Applicant should specifically claim those limitations. Therefore this argument is moot.

31. On pages 3 and 4, Applicant argues in essence:

> *"A person of ordinary skill in the art would not have been motivated to separate the instruction path from the data path in a purely instruction-driven processor as taught by Hennessy, nor in a purely data-driven processor architecture as taught by Arvind et al., nor would their be an advantage to doing so."*

As an initial matter in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413,

208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Furthermore, separating the instruction path from the data path is not only well known and supported by the courts, but it also would have been obvious to one of ordinary skill in the art at the time the invention was made. When the path that instructions travel is a separate from the path that data travels, then when bits are read from a path, no extra coding or tags are necessary to distinguish instructions from data, i.e. instructions are read from an instruction path and data is read from a data path. Furthermore referring to Figure 18 on page 313, there is an arrow from the program memory for the opcode, or instruction, and a separate arrow from the program memory for the data. These separate arrows strongly indicate that instructions and data each have their own separate paths. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instruction path of Arvind be separate from the data path of Arvind, such that no extra coding is necessary to distinguish instructions from data when bits are read from a path. So this case is consistent with the holding that making something separable is not a patentable difference. Therefore this argument is moot.

Conclusion

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

33. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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